REMARKS

The above-referenced application has been reviewed in light of the Examiner's Office Action dated 26 May 2004. The Specification has been amended to better discuss the novelty of the make-links and their construction as depicted in Figures 4 and 6. Claims 1, 3-5, 9-10 and 14-15 have been amended. Claims 6-8 and 11-13 have been canceled, without prejudice. Claims 16-21 have been added. The examiner's indication of allowable subject matter is gratefully acknowledged. No new matter has been added. The Examiner's reconsideration of the rejections in view of the above amendments and the following remarks is respectfully requested.

In accordance with the Office Action, Claims 1-6, 10-11 and 15 stand rejected under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 5,262,994 to McClure, hereinafter McClure. Applicants respectfully submit that amended Claims 1, 3-5, 9-10, 14-15, and original Claim 2 are patentable over McClure for at least the reasons set forth below.

With respect to amended Claims 1 and 15, Applicants respectfully submit that McClure fails to render the claims obvious. McClure does not teach or suggest make-links wherein "...the make-links are formed by at least one conductor in a first layer having its elongated axis disposed at a substantially perpendicular angle relative to at least one conductor in a second layer...". This feature of make-link construction helps make the fuse box of the current application, significantly smaller than those possible with other types of fuses, as depicted by Applicants' Figures 4 and 6 as compared to Applicants' Prior Art Figure 2. Thus, as McClure neither teaches nor suggests the

formation of the make-links on a memory chip, and how this formation can be used to conserve space, McClure fails to render amended Claims 1 and 15 obvious.

With respect to amended Claims 5 and 10 Applicants respectfully submit that McClure fails to render the claims obvious. McClure fails to teach or suggest a redundant address decoder with a "...a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links and a gate connected to said redundancy enable signal line...". Thus, McClure fails to render amended Claims 5 and 10 obvious.

With respect to amended Claims 2-4, 9 and 14 Applicants respectfully submit that McClure fails to teach or suggest each and every element, as set forth in the dependent claims of the current application, for at least the reasons stated below. Claims 1, 5, and 10 are not taught or suggested by McClure. Claims 2-4 depend from Claim 1, Claim 9 depends from Claim 5 and Claim 14 depends from claim 10, necessarily including each of the elements and limitations thereof. Thus, each and every element of Claims 2-4, 9, and 10 are neither taught nor suggested by McClure.

In accordance with the Office Action, Claims 1-6, 10-11 and 15 stand rejected under 35 U.S.C. §103(a), as being unpatentable over Japanese Patent Document No. JP406295594A to Shimizu, hereinafter Shimizu. Applicants respectfully submit that amended Claims 1, 3-5, 9-10, 14-15, and original Claim 2 are patentable over Shimizu for at least the reasons set forth below.

With respect to amended Claims 1 and 15, Applicants respectfully submit that Shimizu fails to render the claims obvious. Shimizu does not teach or suggest make-links wherein "...the make-links are formed by at least one conductor in a first layer having its

elongated axis disposed at a substantially perpendicular angle relative to at least one conductor in a second layer...". This feature of make-link construction helps make the fuse box of the current application, significantly smaller than those possible with other types of fuses, as depicted by Applicants' Figures 4 and 6 as compared to Applicants' Prior Art Figure 2. Thus, as Shimizu neither teaches nor suggests the formation of the make-links on a memory chip, and how this formation can be used to conserve space, Shimizu fails to render amended Claims 1 and 15 obvious.

With respect to amended Claims 5 and 10 Applicants respectfully submit that Shimizu fails to render the claims obvious. Shimizu fails to teach or suggest a redundant address decoder with a "...a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links and a gate connected to said redundancy enable signal line...". Thus, Shimizu fails to render amended Claims 5 and 10 obvious.

With respect to amended Claims 2-4, 9 and 14 Applicants respectfully submit that Shimizu fails to teach or suggest each and every element, as set forth in the dependent claims of the current application, for at least the reasons stated below. Claims 1, 5, and 10 are not taught or suggested by Shimizu. Claims 2-4 depend from Claim 1, Claim 9 depends from Claim 5 and Claim 14 depends from claim 10, necessarily including each of the elements and limitations thereof. Thus, each and every element of Claims 2-4, 9, and 10 are neither taught nor suggested by Shimizu.

In accordance with the Office Action, Claims 1-6, 10-11and 15 stand rejected under 35 U.S.C. §103(a), as being unpatentable over Japanese Patent Document No. JP02000012699A to Mi et. al., hereinafter Mi. Applicants respectfully submit that

amended Claims 1, 3-5, 9-10, 14-15, and original Claim 2 are patentable over Mi for at least the reasons set forth below.

With respect to amended Claims 1 and 15, Applicants respectfully submit that Mi fails to render the claims obvious. Mi does not teach or suggest make-links wherein "...the make-links are formed by at least one conductor in a first layer having its elongated axis disposed at a substantially perpendicular angle relative to at least one conductor in a second layer...". This feature of make-link construction helps make the fuse box of the current application, significantly smaller than those possible with other types of fuses, as depicted by Applicants' Figures 4 and 6 as compared to Applicants' Prior Art Figure 2. Thus, as Mi neither teaches nor suggests the formation of the make-links on a memory chip, and how this formation can be used to conserve space, Mi fails to render amended Claims 1 and 15 obvious.

With respect to amended Claims 5 and 10 Applicants respectfully submit that Mi fails to render the claims obvious. Mi fails to teach or suggest a redundant address decoder with a "...a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links and a gate connected to said redundancy enable signal line...". Thus, Mi fails to render amended Claims 5 and 10 obvious.

With respect to amended Claims 2-4, 9 and 14 Applicants respectfully submit that Mi fails to teach or suggest each and every element, as set forth in the dependent claims of the current application, for at least the reasons stated below. Claims 1, 5, and 10 are not taught or suggested by Mi. Claims 2-4 depend from Claim 1, Claim 9 depends from Claim 5 and Claim 14 depends from claim 10, necessarily including each of the elements

and limitations thereof. Thus, each and every element of Claims 2-4, 9, and 10 are neither taught nor suggested by Mi.

In accordance with the Office Action, Claims 7-9 and 12-14 contain allowable subject matter, if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants submit that new independent Claim 16 was created by copying parent Claims 5-6 into Claim 7. New dependent Claims 17-18, now depending from Claim 16, were created by copying the original dependent Claims 8-9 respectively.

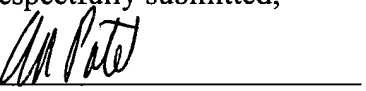
New independent Claim 19 was created by copying parent Claims 10-11 into Claim 12. New dependent Claims 20-21 were created by copying original dependent Claims 13-14 respectively.

Thus, Claims 16-21 contain no new matter and are in condition for allowance.

Conclusion

Accordingly, it is respectfully submitted that amended independent Claims 1, 5, 10 and 15, as well as new independent Claims 16 and 19, are in condition of allowance for at least the reasons stated above. Since Claims 2-4, 9, 14, 17-18 and 20-21 each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated. Thus, each of Claims 1-5, 9-10 and 14-21 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully submitted,



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